What is claimed is:

1. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of an input signal and a first feedback (FB) unit to eliminate a post-ghost of the input signal;

a Trellis decoder for Trellis-decoding an output signal of the first equalizer; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal and a second FB unit to eliminate the post-ghost of the input signal based on an output signal of the Trellis decoder.

2. The channel equalizer as claimed in claim 1, further comprising a buffer to store the input signal, input to the first equalizer, for a certain period of time.

3. The channel equalizer as claimed in claim 1, wherein the Trellis decoder has an entire decoding depth of N and an entire traceback delay symbol length of $N \times K$, with N and K being natural numbers.

4. The channel equalizer as claimed in claim 1, further comprising a first error calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit.

5. The channel equalizer as claimed in claim 4, further comprising a Trellis controller to control the Trellis decoder to output to the first FB unit an estimation signal outputted in a predetermined decoding depth state of the Trellis decoder if the first equalization error value becomes less than or equal to a threshold value.

6. The channel equalizer as claimed in claim 5, wherein an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n \times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number and $n \leq N$.

7. The channel equalizer as claimed in claim 4, further comprising a Trellis controller to control the Trellis decoder to output to the first FB unit plural estimation signals output in plural states of the entire decoding depths of the Trellis decoder, if the first equalization error value becomes less than or equal to a threshold value.

8. The channel equalizer as claimed in claim 7, wherein an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n\times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number, with $n \leq N$, and with the plural estimation signals output in the plural states being output to corresponding filter taps of the first FB unit, respectively.

9. The channel equalizer as claimed in claim 1, further comprising a second error calculation unit to calculate a second equalization error value based on the output signal of the Trellis decoder.

10. A channel equalization method for a signal-carrier receiver, comprising:

first equalizing an input signal by eliminating pre-ghost and post-ghost of the input signal using a first feed forward (FF) unit and a first feedback (FB) unit;

Trellis-decoding a result of the first equalizing of the input signal; and

second equalizing a result of the Trellis-decoding, comprising eliminating the pre-ghost of the input signal in a second FF unit and eliminating the post-ghost of the input signal in a second FB unit based on the the result of the Trellis-decoding.

11. The channel equalization method as claimed in claim 10, further comprising storing the input signal for a certain period of time.

12. The channel equalization method as claimed in claim 10, wherein the Trellis decoder has an entire decoding depth of N and an entire traceback delay symbol length of $N\times K$, with N and K being natural numbers.

13. The channel equalization method as claimed in claim 10, wherein the first equalizing further comprises first error calculating for calculating a first equalization error value based on a signal resulting from the addition of an output signal of the first FF unit and an output signal of the first FB unit.

14. The channel equalization method as claimed in claim 13, further comprising feedback by outputting to the first FB unit an estimation signal output in a predetermined decoding depth state of the Trellis decoder if the first equalization error value becomes less than or equal to a threshold value.

15. The channel equalization method as claimed in claim 14, wherein, in the feedback, an estimation signal output in a state of decoding depth n ($n \leq N$) of the Trellis decoder is output to a $\{1+(n\times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number and with $n \leq N$.

16. The channel equalization method as claimed in claim 13, further comprising feedback by outputting to the first FB unit plural estimation signals output in plural states of the entire decoding depths of the Trellis decoder, if the first equalization error value becomes less than or equal to a threshold value.

17. The channel equalization method as claimed in claim 16, wherein, in the feedback, an estimation signal output in a state of decoding depth n ($n \leq N$) of the Trellis decoder is output to a $\{1+(n\times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number, with $n \leq N$, and with the plural estimation signals output in the plural states being output to corresponding filter taps of the first FB unit, respectively.

18. The channel equalization method as claimed in claim 10, wherein the second equalization further comprises second error calculating for calculating a second equalization error value based on the Trellis-decoding result.

19. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first FF unit to eliminate a pre-ghost of an input signal, a first FB unit to eliminate a post-ghost of the input signal, and a first error calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit;

a buffer to store the input signal input to the first equalizer for a certain period of time;

a Trellis decoder having an entire decoding depth of N and an entire traceback delay symbol length of $N\times K$, with N and K being natural numbers, and Trellis-decode an output signal of the first equalizer;

a Trellis controller to control the Trellis decoder to output to the first FB unit an estimation signal output in a predetermined decoding depth state of the Trellis decoder if the first equalization error value becomes less than or equal to a threshold value; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal output from the buffer and a second FB unit to eliminate the post-ghost of the input signal based on an output of the Trellis decoder.

20. The channel equalizer as claimed in claim 19, wherein the estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n\times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number and with $n \leq N$.

21. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of an input signal, a first feedback (FB) unit to eliminate a post-ghost of the input signal, and a first error calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit;

a buffer to store the input signal input to the first equalizer for a certain period of time;

a Trellis decoder having an entire decoding depth of N and an entire traceback delay symbol length of $N\times K$, with N and K being natural numbers, and Trellis-decode an output signal of the first equalizer;

a Trellis controller to control the Trellis decoder to output to the first FB unit plural estimation signals output in plural states of entire decoding depths of the Trellis decoder, if the first equalization error value becomes less than or equal to a threshold value; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal output from the buffer and a second FB unit to eliminate the post-ghost of the input signal, based on an output of the Trellis decoder.

22. The channel equalizer as claimed in claim 21, wherein an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n\times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number, with $n \leq N$, and with the plural estimation signals output in the plural states being output to corresponding filter taps of the first FB unit, respectively.

23. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of an input signal, and a first feedback (FB) unit to eliminate a post-ghost of the input signal;

a buffer to store the input signal input to the first equalizer for a certain period of time;

a Trellis decoder having a decoding depth of N and an entire traceback delay symbol length of $N \times K$, with N and K being natural numbers, and to Trellis-decode an output signal of the first equalizer; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal output from the buffer, a second FB unit to eliminate the post-ghost of the input signal based on an output of the Trellis decoder, and a second error calculation unit to calculate a second equalization error value based on the output of the Trellis decoder.

24. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of an input signal, a first feedback (FB) unit to eliminate a post-ghost of the input signal, and a first error calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit;

a buffer for storing the input signal input to the first equalizer for a certain period of time;

a Trellis decoder having an entire decoding depth of N and an entire traceback delay symbol length of $N \times K$, with N and K being, and Trellis-decode an output signal of the first equalizer;

a Trellis controller to control the Trellis decoder to output to the first FB unit an estimation signal output in a predetermined decoding depth state of the Trellis decoder if the first equalization error value becomes less than or equal to a threshold value; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal output from the buffer, a second FB unit to eliminate the post-ghost of the input signal based on an output of the Trellis decoder, and a second error calculation unit to calculate a second equalization error value based on the output of the Trellis decoder.

25. The channel equalizer as claimed in claim 24, wherein an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n \times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number and with $n \leq N$.

26. A channel equalizer for a single-carrier receiver, comprising:

a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of an input signal, a first feed back (FB) unit to eliminate a post-ghost of the input signal, and a first error

calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit;

a buffer to store the input signal input to the first equalizer for a certain period of time;

a Trellis decoder having an entire decoding depth of N and an entire traceback delay symbol length of $N \times K$, with N and K being natural numbers, and to Trellis-decode an output signal of the first equalizer;

a Trellis controller to control the Trellis decoder to input to the first FB unit plural estimation signals output in plural states of the entire decoding depths of the Trellis decoder, if the first equalization error value becomes less than or equal to a threshold value; and

a second equalizer having a second FF unit to eliminate the pre-ghost of the input signal output from the buffer, a second FB unit to eliminate the post-ghost of the input signal based on an output of the Trellis decoder, and a second error calculation unit to calculate a second equalization error value based on the output of the Trellis decoder.

27. The channel equalizer as claimed in claim 26, wherein an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n \times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number, with $n \leq N$, and with the plural estimation signals output in the plural states are output to corresponding filter taps of the first FB unit, respectively.

28. A receiver, comprising:

a demodulator to convert a received signal to a baseband signal;

a channel equalizer to compensate for channel distortions in the demodulated received signal;

a phase recovery unit to recover a phase of the channel equalized signal; and

a decoder to decode the phase recovered signal,

wherein the channel equalizer further comprises a first equalizer having a first feed forward (FF) unit to eliminate a pre-ghost of a channel equalizer input signal and a first feedback (FB) unit to eliminate a post-ghost of the channel equalizer input signal, a Trellis decoder to Trellis-decode an output signal of the first equalizer, and a second equalizer having a second FF unit to eliminate the pre-ghost of the channel equalizer channel equalizer signal and a second FB unit to eliminate the post-ghost of the channel equalizer input signal based on an signal decoded by the Trellis decoder.

29. The receiver as claimed in claim 28, wherein the channel equalizer further comprises a buffer to store the input signal, input to the first equalizer, for a certain period of time.

30. The receiver as claimed in claim 29, wherein, in the channel equalizer, the Trellis decoder has an entire decoding depth of N and an entire traceback delay symbol length of $N \times K$, with N and K being natural numbers.

31. The receiver as claimed in claim 1, wherein the channel equalizer further comprises a first error calculation unit to calculate a first equalization error value based on an added signal of an output signal of the first FF unit and an output signal of the first FB unit.

32. The receiver as claimed in claim 31, wherein the channel equalizer further comprises a Trellis controller to control the Trellis decoder to output to the first FB unit an estimation signal outputted in a predetermined decoding depth state of the Trellis decoder if the first equalization error value becomes less than or equal to a threshold value.

33. The receiver as claimed in claim 32, wherein, in the channel equalizer, an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n \times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number and $n \leq N$.

34. The receiver as claimed in claim 31, wherein the channel equalizer further comprises a Trellis controller to control the Trellis decoder to output to the first FB unit plural estimation signals output in plural states of the entire decoding depths of the Trellis decoder, if the first equalization error value becomes less than or equal to a threshold value.

35. The channel equalizer as claimed in claim 34, wherein, in the channel equalizer, an estimation signal output in a state of decoding depth n of the Trellis decoder is output to a $\{1+(n \times K)\}^{th}$ filter tap of the first FB unit, with n being a natural number, with $n \leq N$, and with the plural estimation signals output in the plural states being output to corresponding filter taps of the first FB unit, respectively.

36. The channel equalizer as claimed in claim 28, wherein the channel equalizer, further comprises a second error calculation unit to calculate a second equalization error value based on the output signal of the Trellis decoder.

37. A receiver comprising a demodulator, a phase recovery unit, a decoder to decode the phase recovered signal, and a channel equalizer to compensate for channel distortions in the demodulated received signal according to the method of claim 10.

38. A receiver comprising a demodulator, a phase recovery unit, a decoder, and a channel equalizer, to compensate for channel distortions in a demodulated received signal, according to claim 19.

39. A receiver comprising a demodulator, a phase recovery unit, a decoder, and a channel equalizer to compensate for channel distortions in a demodulated received signal, according to claim 21.

40. A receiver comprising a demodulator, a phase recovery unit, a decoder, and a channel equalizer, to compensate for channel distortions in a demodulated received signal, according to claim 23.

41. A receiver comprising a demodulator, a phase recovery unit, a decoder, and a channel equalizer, to compensate for channel distortions in a demodulated received signal, according to claim 24.

42. A receiver comprising a demodulator, a phase recovery unit, a decoder, and a channel equalizer, to compensate for channel distortions in a demodulated received signal, according to claim 26.